DUAL DIFFERENTIAL COMPARATOR CIRCUIT WITH FULL RANGE OF INPUT SWING

FIELD OF THE INVENTION

[0001] The present invention relates to a dual differential comparator circuit, and more particularly relates to a dual differential comparator circuit with full range of input swing employed in a transmitting terminal of the Universal Serial Bus (USB) as an input differential receiver.

BACKGROUND OF THE INVENTION

[0002] The Universal Serial Bus (USB) is a kind of interfaces of the peripheral equipment, and is set up jointly by seven manufacturers of software and hardware. The transmitting speed of this kind of interfaces can be either 1.5 Mbps or 12 Mbps, and can be connected to up to 127 sets of peripheral equipment simultaneously.

[0003] Since there is a very restricted regulation regarding the voltage range capable of receiving the input signals V_{in} for the Universal Serial Bus (USB), all voltage values within a certain range (0.8 to 2.2V) should be capable of being received satisfactorily.

[0004] Please refer to Figs. 1(a) and 1(b), which are the circuits employed for receiving the input signals traditionally. In Fig 1(a), a NMOS is employed for receiving input signals within a voltage range having relatively higher values. In Fig 1(b), a PMOS, with characteristics opposite to the NMOS, is employed for receiving input signals within a voltage range having relatively lower values. The circuits in Figs 1(a) and 1(b) are capable of receiving input voltage V_{in} which is restricted to relatively higher and lower voltage values, and the range of voltage values is also relatively smaller.

[0005] But the desired voltage range of the input signals that the Universal Serial Bus (USB) is capable of receiving is getting larger and larger now, the circuits employed traditionally could not meet such a challenge. The manufacturers are all trying their best to combined the PMOS with the NMOS so as to enlarge the voltage range of the input signals that the Universal Serial Bus (USB) is capable of receiving.

[0006] Please refer to Fig 2, it shows a receiving circuit which is a combination of PMOS and NMOS so as to enlarge the voltage range of the input signals. When the input voltage belongs to a relatively lower voltage, the PMOS transistors M5 and M6 receive the input voltage and transmit it to a 1:1 tail-current transistor 20 so as to produce and to output a tail-current. If the input voltage belongs to a relatively higher voltage, the NMOS transistors M1 and M2 receive the input voltage and transmit it to a 1:1 tail-current transistor 21 so as to produce and to output a tail-current.

[0007] Though the circuit in Fig. 2 can be employed so as to enlarge the voltage range of input signals, but the tail-current transistors 20 and 21 are always in conducting and their status won't be dynamically changed following the "shut down" "turn on" of the PMOS or NMOS respectively. No matter the transmitting signals are received by which, either a PMOS or a NMOS, there is a tail-current transistor in conducting but not operated so as to increase the power loss.

[0008] Besides, the PMOS and the NMOS are conducted simultaneously when the input voltage belongs to the central portion of the voltage range which will result in a relatively higher than normal tail-current so as to cause an extremely high power loss.

[0009] Keep the drawbacks of the prior art in mind, and employ experiments and research full-heartily and persistently, a dual differential comparator circuit with full range of input swing is finally conceived by the applicants.

SUMMARY OF THE INVENTION

[0010] It is therefore an object of the present invention to provide a dual differential comparator circuit with full range of input swing so as to be employed in a transmitting terminal of the Universal Serial Bus (USB) as an input differential receiver.

[0011] According to the aspect of the present invention, the differential comparator circuit for receiving an input voltage within a pre-determined range, amplifying the input voltage into an output voltage, and outputting the output voltage, wherein the range includes a first range portion and a second range portion, and the input voltage ranged in the first range portion is higher than that ranged in the second range portion, includes: a first differential comparator for receiving and amplifying the input voltage within the first range portion, and outputting the output voltage, a detecting circuit electrically connected to the first differential comparator for producing a trigger signal when the detecting circuit detects that the first differential comparator is shut down due to the fact that the input voltage is lower than a lower-limit of the first range portion, and a second differential comparator electrically connected to the detecting circuit for receiving and amplifying the input voltage within the second range portion, and outputting the output voltage in response to the trigger signal.

[0012] Preferably, the differential comparator circuit is employed in a transmitting terminal of a Universal Serial Bus (USB).

[0013] Preferably, the first differential comparator further includes: a first differential receiving circuit for receiving the input voltage within the first range portion, and a first operational amplifier circuit electrically connected to the first differential receiving circuit for amplifying the input voltage received by the first differential receiving circuit and generating the output voltage.

[0014] Preferably, the second differential comparator further includes: a second differential receiving circuit electrically connected to the detecting circuit for receiving the input voltage ranged in the second range portion in response to the trigger signal, and a second operational amplifier circuit electrically connected to the second differential receiving circuit for amplifying the input voltage received by the second differential receiving circuit and generating the output voltage.

[0015] Preferably, the differential comparator circuit further includes an output circuit for outputting the output voltage.

[0016] Preferably, the second differential comparator is shut down to avoid a floating when the first differential comparator is operated.

[0017] Preferably, the first differential comparator is shut down when the second differential comparator is operated.

[0018] According to another aspect of the present invention, the differential comparator circuit for receiving an input voltage within a pre-determined range, amplifying the input voltage into an output voltage, and outputting the output voltage, wherein the range includes a first range portion and a second range portion, and the input voltage ranged in the first range portion is higher than that ranged in the second range portion, includes: a first differential receiving circuit for receiving the input voltage ranged in

the first range portion, a first operational amplifier circuit electrically connected to the first differential receiving circuit for amplifying the input voltage received by the first differential receiving circuit and generating the output voltage, a detecting circuit electrically connected to the first differential receiving circuit for producing a trigger signal when the detecting circuit detects the first differential receiving circuit is shut down due to the fact that the input voltage is lower than a lower-limit of the first range portion, a second differential receiving circuit electrically connected to the detecting circuit for receiving the input voltage ranged in the second range portion in response to the trigger signal, and a second operational amplifier circuit electrically connected to the second differential receiving circuit for amplifying the input voltage received by the second differential receiving circuit and generating the output voltage.

[0019] Preferably, the differential comparator circuit further includes an output circuit for outputting the output voltage.

[0020] Preferably, the second differential receiving circuit is shut down to avoid a floating when the first differential receiving circuit and the first operational amplifier circuit are operated.

[0021] Preferably, the first differential receiving circuit and the first operational amplifier circuit are shut down when the second differential receiving circuit and the second operational amplifier circuit are operated.

[0022] According to another aspect of the present invention, the differential comparator circuit for receiving an input voltage within a pre-determined range, amplifying the input voltage into an output voltage, and outputting the output voltage, wherein the range includes a first range portion and a second range portion, and the input voltage ranged in the first

portion is higher than that ranged in the second range portion, includes: a first differential receiving circuit for receiving the input voltage ranged in the first range portion, a detecting circuit electrically connected to the first differential receiving circuit for producing a trigger signal when the detecting circuit detects that the first differential receiving circuit is shut down due to the fact that the input voltage is lower than a lower-limit of the first range portion, and a second differential receiving circuit electrically connected to the detecting circuit for receiving the input voltage ranged in the second range portion in response to the trigger signal.

[0023] The present invention may best be understood through the following descriptions with reference to the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Figs. 1(a) to 1(b) are the schematic diagrams showing the circuits for receiving input signals of the prior art of the present invention;

[0025] Fig. 2 is a schematic circuit diagram showing the circuit with combined PMOS and NMOS for receiving input signals of the prior art of the present invention;

[0026] Fig. 3 is a block diagram showing the most preferred embodiment of the present invention; and

[0027] Fig. 4 is a circuit diagram showing the most preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0028] Please refer to Figs. 3 and 4, which are the block diagram and circuit diagram showing the most preferred embodiment of the present invention respectively.

[0029] A dual differential comparator circuit with full range of input swing of the present invention is employed in a transmitting terminal of the Universal Serial Bus (USB) as an input differential receiver for receiving all input signals within the voltage range of 0 to V_{dd} (about 0 to 3.3V), amplifying the input signals, and outputting an output voltage. Therein, the voltage range can be further divided into a first portion with a higher voltage (about 2 to 3.3V), and a second portion with a lower voltage (about 0 to 2V). Please refer to Fig. 3, the above-mentioned circuit of the present invention includes: a detecting circuit 30, a first differential comparator circuit 31, a second differential comparator circuit 32, and an output circuit 33.

[0030] Please refer to Fig. 4, the input signals with the input voltages about 2 to 3.3Volt are received by the first differential comparator circuit 31 through the first differential receiving circuit 311, the received input voltages are amplified by the first operational amplifier 312 electrically connected to the first differential receiving circuit 311, and the output voltages are produced and output through the output circuit 33.

[0031] The detecting circuit 30, electrically connected to the first differential receiving circuit 311, is mainly employed to detect the operational status of the first differential receiving circuit 311 (detecting at the marked place of "a" as shown in Fig. 4). When the first differential receiving circuit 311 is under a receiving status, a stop signal is produced to shut down the second differential comparator circuit 32 to avoid the power loss. When the first differential receiving circuit 311 is shut down due to the voltage of input signal is within the 0 to 2Volt voltage range and is detected, a trigger signal is produced to drive the second differential comparator 32 for receiving the input signals.

[0032] After the second differential comparator 32 is driven by the trigger signal, the input signals each with an input voltage of 0 to 2Volt are received by the second differential receiving circuit 321, the received voltages are amplified by the second operational amplifier 322 which is electrically connected to the second differential receiving circuit 321, and the output voltages are produced and output through the output circuit 33.

[0033] Therein, the first differential receiving circuit includes a NMOS with two receiving terminals (IN+ and IN-). When the voltage values of IN+ > IN-, the output voltage is output at a higher level of V_{dd}. When the voltage values of IN+ < IN-, the output voltage is output at a lower level of 0. The output voltage mentioned above is varied according to which one of the two values of IN+ and IN- is relatively larger or smaller.

[0034] The second differential receiving circuit 321 includes a NMOS and a PMOS with two receiving terminals (IN+ and IN-) and a level shift circuit 3211 so as to avoid the floating and to gain the cumulative effect. Regarding the PMOS, the output voltage is output at a higher level of V_{dd} when the voltage values of IN+ > IN-. Regarding the PMOS, the output voltage is output at a lower level of 0 when the voltage values of IN+ < IN-. The output voltage mentioned above is varied according to which one of the two values of IN+ and IN- is relatively larger or smaller.

[0035] Please refer to Fig. 4, the second differential receiving circuit 321 will be shut down when the receiving voltages of IN+ and IN- are too high. Therein, the level shift circuit 3211 can be employed to amplify the receiving input signals initially and to shut down the two receiving terminals when the stop signal is generated by the detecting circuit 30.

[0036] In conclusion, the dual differential comparator circuit of the present invention would effectively guarantee the differential comparator not in use would be shut down totally through the detecting circuit so as to improve the drawbacks of the prior art regarding the power loss with a common mode range of 0 to Vdd, the resolution can reach 50 to 200 mV (currently the desired value of USB 1.1 version is 200mV), and the maximum delay time is 7 ns. According to the real simulation results mentioned above, the results of the present invention are better than the specification of the USB 1.1 version. Thus, the present invention has its value in the industry, and the purpose of developing the present invention is achieved.

[0037] While the invention has been described in terms of what are presently considered to be the most practical and preferred embodiments, it is to be understood that the invention need not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures. Therefore, the above description and illustration should not be taken as limiting the scope of the present invention which is defined by the appended claims.